Code No.

Symbol Number: _____ Invigilator's Sign: _____ Superintendent's Sign: _____

Symbol No. in Words: _____

Faculty: Engineering **Level: Bachelor** **Exam Year:2080 Mangsir** **Year/Part :II/I**

Program: Electrical and Electronics **Subject: Logic Circuit (EG502EX)**

GROUP A (Multiple Choice Questions) **[10x1=10]**

i. Answers should be given by filling the Objective Answer Sheet.
ii. Rough can be done in the main answer sheet
iii. Maximum time of 20 minutes within the total time is given for this group

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1. The gray code conversion of 11010_2 is:
a. 10011_2 b. 10111_2
c. 00101_2 d. 00110_2

2. In a NAND gate, the output is high when …… .
a. All the inputs are low b. All the inputs are high
c. Any one input is low d. Any one input is high

3. In Boolean algebra, A+ A'B is equal to:
a. 0 b. A
c. B d. A+B

4. The number of inputs and outputs of a full adder circuit are:
a. 2 and 2 b. 2 and 3
c. 3 and 2 d. 3 and 3

5. Which of the following binary number has even parity?
a. 1101101_2 b. 1101010_2
c. 10010100_2 d. 0110111_2

6. In a JK Flip Flop, if J=K=1, what will be the output of the flip-flop?
a. $Q_{n+1} = 0$ b. $Q_{n+1} = 1$
c. $Q_{n+1} = Q_n$ d. $Q_{n+1} = Q_n'$

7. We need at least …… flip-flops to design a Mod-10 counter.
a. 1 b. 2
c. 3 d. 4

8. For a down counter, the next output after 1000_2 will be:
a. 1001_2 b. 0000_2
c. 0111_2 d. 1111_2

9. The number of states for a 2-bit gray code sequential circuit will be:
a. 2 b. 3
c. 4 d. 8

10. In a 4-bit Register, if the inputs are sent one bit at each clock pulse and the output is taken all 4-bits at a single clock pulse, then the register is ……
a. PISO b. SIPO
c. PIPO d. SISO

Multiple Choice Questions' Answer Sheet

Code No. _____ Marks Secured: _____

In Words: _____

Examiner's Sign: _____ Date: _____

Scrutinizer's Marks: _____

In Words: _____

Scrutinizer's Sign: _____ Date: _____

Corrected Fill: Ⓐ ● Ⓒ Ⓓ

Incorrected Fill: ~~Ⓐ~~ Ⓑ ● Ⓓ ✓

1.	Ⓐ	Ⓑ	Ⓒ	Ⓓ	6.	Ⓐ	Ⓑ	Ⓒ	Ⓓ
2.	Ⓐ	Ⓑ	Ⓒ	Ⓓ	7.	Ⓐ	Ⓑ	Ⓒ	Ⓓ
3.	Ⓐ	Ⓑ	Ⓒ	Ⓓ	8.	Ⓐ	Ⓑ	Ⓒ	Ⓓ
4.	Ⓐ	Ⓑ	Ⓒ	Ⓓ	9.	Ⓐ	Ⓑ	Ⓒ	Ⓓ
5.	Ⓐ	Ⓑ	Ⓒ	Ⓓ	10.	Ⓐ	Ⓑ	Ⓒ	Ⓓ

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Faculty: Engineering	**Exam Year:2080 Mangsir**	**Year/Part: II/I**
Program: Electrical and Electronics	**Level: Bachelor**	**F.M.: 50**
Subject: Logic Circuit (EG502EX)	**Time: 3 Hours**	**P.M.: 20**

- ✓ *Group A contains Multiple Choice Questions of 10 marks.*
- ✓ *Candidates are required to give their answers in their own words as far as practicable.*
- ✓ *The figures in the margin indicate Full Marks.*
- ✓ *Assume suitable data if necessary*.

Group 'B'
Short Answer Questions (Attempt any EIGHT questions only.) (8×2=16)

1. Subtract using 2's complement method.
$1101010_2 - 1010111_2$
2. Convert into the given form:
a) FF_{16} to Octal b) 1011101_2 to Gray Code
3. Realize the circuit of AND gate using NOR gate only.
4. Prove that (using Boolean algebra): $A.B+\bar{A}C = (\bar{A}+C)(A+B)$
5. Draw the truth table and logic circuit of 8:1 Multiplexer.
6. Draw the truth table and logic circuit of a Half Subtractor circuit.
7. Draw the circuit diagram and excitation table of a NAND gated SR Flip Flop.
8. Draw the circuit diagram of 4-bit Ring Counter.
9. Realize NAND gate using TTL Logic.

Group 'C'

Long Answer Questions (Attempt any SIX questions only.)(6×4=24)

10. Simplify using K-Map for $\sum(1,2,3,8,9,10,11,14) + \sum d\ (0,4,12)$ and write the expression in Sum-of-Products form.
11. Realize the logic circuit for 1-bit magnitude comparator.
12. Realize a T flip-flop using D flip-flop.
13. Design a decade counter using T flip-flop.
14. Explain SISO register with logic circuit and timing diagram.
15. Design a sequential machine that has serial input X and output Z. The output Z will be 1 only when the sequence of inputs is 10102. Use T Flip-flop for the design.
16. Realize the circuit for CMOS NAND Gate.

∞∞***All the Best*** ∞∞